

AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A voltage generating circuit comprising:

a first transistor which allows a first current to flow in an emitter thereof;

a second transistor which allows a second current ~~which~~ has having a current density larger than a current density of the emitter of the first transistor to flow in an emitter thereof;

a first resistance which is provided between the emitter of the first transistor and the emitter of the second transistor;

a second resistance which is provided between the emitter of the second transistor and a ground potential of the voltage generating circuit;

a third resistance which is provided between a collector of the first transistor and a power source voltage;

,

a fourth resistance which is provided between a collector of the second transistor and the power source voltage; and

a differential amplifier circuit having ~~the~~ a CMOS constitution which forms an output voltage upon receiving a collector voltage of the first transistor and a collector voltage of the second transistor, ~~and, at the same time,~~ which supplies the output voltage to bases of the first transistor and the second transistor in common,

wherein the first transistor and the second transistor are constituted by making ~~us~~ use of a semiconductor region formed in a CMOS process associated with ~~of a CMOS circuit which constitutes~~ the differential amplifier circuit.

2. (Original) A voltage generating circuit according to claim 1, wherein the third resistance and the fourth resistance are configured to possess a same resistance value.

3. (Original) A voltage generating circuit according to claim 2, wherein an emitter area of the first transistor is set larger than an emitter area of the second transistor.

4. (Cancelled)

5. (Currently Amended) A semiconductor integrated circuit device including a reference voltage generating circuit, the reference voltage generating circuit comprising:~~which comprises:~~

a first transistor which allows a first current to flow in an emitter thereof;

a second transistor which allows a second current ~~which has~~having a current density larger than a current density of the emitter of the first transistor to flow in an emitter thereof;

a first resistance which is provided between the emitter of the first transistor and the emitter of the second transistor;

a second resistance which is provided between the emitter of the second transistor and a first external terminal which supplies a ground potential of the circuit;~~which is supplied from an external terminal;~~

a third resistance which is provided between a collector of the first transistor and a second external terminal which supplies a power source voltage;~~which is supplied from an external terminal;~~

a fourth resistance which is provided between a collector of the second transistor and the ~~power source~~ voltage second external terminal; and

a differential amplifier circuit having ~~the~~ a CMOS constitution which forms an output voltage upon receiving a collector voltage of the first transistor and a collector voltage of the second transistor, ~~and, at the same time,~~ which supplies the output voltage to bases of the first transistor and the second transistor in common,

wherein the first transistor and the second transistor are constituted by ~~making use of~~ using a semiconductor region formed in a CMOS process ~~of a CMOS circuit which constitutes associated with~~ the differential amplifier circuit.

6. (Currently Amended) A semiconductor integrated circuit device according to claim 5, ~~wherein the semiconductor integrated circuit device which~~ includes a CMOS circuit ~~which is constituted of~~ having a second conductive-type well region and a first conductive-type well region ~~which are~~ formed on a first conductive-type semiconductor substrate, a first conductive-type MOSFET ~~which is~~ formed on the second conductive-type well region,

and a second conductive-type MOSFET ~~which is formed on the~~
first conductive-type well region, ~~and~~

wherein each of the first transistor and the second
transistor which constitute of the reference voltage
generating circuit are is formed of a bipolar transistor
having the a lateral structure which uses with collector,
emitter, and base portions being constituted by diffusion
layers which are formed on respective portions of a first
conductive-type well arrangement, the diffusion layers of
the collector and emitter portions being formed in a step
for forming source and drain diffusion layers of the second
conductive-type MOSFET. ~~which constitutes the CMOS circuit~~
~~as the collector and the emitter and is operated using the~~
~~first conductive-type well region on which the diffusion~~
~~layers which constitute the collector and the emitter are~~
~~formed as a base.~~

7. (Currently Amended) A semiconductor integrated
circuit device according to claim 5, ~~wherein the~~
~~semiconductor integrated circuit device which includes the a~~
CMOS circuit ~~which is constituted of the having a second~~
conductive-type well region and ~~the a first conductive-type~~
well region ~~which are formed on the a first conductive-type~~
semiconductor substrate, ~~the a first conductive-type MOSFET~~

~~which is~~ formed on the second conductive-type well region,
and ~~a the~~ second conductive-type MOSFET ~~which is~~ formed on
the first conductive-type well region, and

wherein the second conductive-type well region ~~having a~~
~~depth for electrically separating~~ separates the first
conductive-type well region on which the second conductive-
type MOSFET is formed from the first conductive-type
semiconductor substrate, and

wherein each of the first transistor and the second
transistor ~~are~~ is formed of a bipolar transistor having ~~the~~
a vertical structure which with ~~uses a second conductive~~
conductive-type diffusion layer, which is formed in a step
for forming source and drain diffusion layers of the ~~first~~
second conductive-type MOSFET, ~~which constitutes the CMOS~~
~~circuit as the~~ as an emitter portion, ~~uses the with a~~
portion of a first conductive-type well-region arrangement,
on which the second conductive-type diffusion layer ~~which~~
~~constitutes~~ constituting the emitter portion is formed, as a
base portion, and ~~uses the with a portion of a second~~
conductive-type well arrangement, ~~region having a depth~~
~~which is provided for which~~ electrically separating
separates said portion of the first conductive-type well
arrangement region which constitutes the base from the first

~~conductive-conductive-type~~ semiconductor substrate, as a collector portion.

8. (Currently Amended) A semiconductor integrated circuit device according to claim 5, ~~wherein the semiconductor integrated circuit device includes which includes~~ a CMOS circuit ~~which is constituted of having~~ a second conductive-type well region and a first conductive-type well region ~~which are formed~~ on a second conductive-type semiconductor substrate, a first conductive-type MOSFET ~~which is formed~~ on the second conductive-type well region, and a second conductive-type MOSFET ~~which is formed~~ on the first conductive-type well region, and

wherein each of the first transistor and the second transistor which constitute of the reference voltage generating circuit are is formed of a bipolar transistor having ~~the a~~ lateral structure ~~which uses with collector, emitter, and base portions being constituted by diffusion layers which are formed on respective portions of a first conductive-type well arrangement, the diffusion layers of the collector and emitter portions being formed in a step for forming source and drain diffusion layers of the second conductive-type MOSFET, which constitutes the CMOS circuit as the collector and the emitter and is operated using the~~

~~first conductive-type well region on which the diffusion layers which constitute the collector and the emitter are formed as a base.~~

9. (Currently Amended) A semiconductor integrated circuit device according to claim 6,

wherein the first conductive-type is a p-type and the second conductive-type is an n-type, and

wherein the ~~[[a]] power source voltage which is~~
supplied from the second external terminal is ~~[[a]]~~
positive. ~~power source voltage.~~

10. (Currently Amended) A semiconductor integrated circuit device according to claim 9,

wherein the second transistor is constituted ~~of~~ by one
unit transistor, and

wherein the first transistor is constituted by
connecting a plurality of unit transistors corresponding to
the second transistor in parallel.

11. (Currently Amended) A semiconductor integrated circuit device according to claim 10,

wherein the first transistor is configured such that
the plurality of unit transistors are formed on portions of

the first conductive-type well regions arrangement having the same depth., and

~~one of the plurality of unit transistors which are formed to have the same constitution as the first transistor is used as the second transistor.~~

12. (Currently Amended) A semiconductor integrated circuit device according to claim 11, ~~wherein the semiconductor integrated circuit device further includes:~~comprising:

a power source circuit which generates an internal voltage, different from ~~[[a]]~~ the power source voltage ~~which is supplied from the~~ second external terminal, upon receiving based on a reference voltage formed by from the reference voltage generating circuit;

an internal circuit which is operated by the power source circuit;

an input circuit which is operated ~~upon receiving a~~ based on the power source voltage supplied from the second external terminal, performs to perform a level conversion ~~upon receiving of~~ an input signal supplied from ~~an~~ a third external terminal and to transmit transmits the converted input signal to the internal circuit; and

an output circuit which is operated ~~upon receiving~~
~~abased on the~~ power source voltage supplied from the second
external terminal, ~~performs~~ to perform a level conversion
~~upon receiving of~~ a signal generated by the internal
circuit[,] and to form ~~forms~~ an output signal to be
outputted from the third external terminal,

wherein the differential amplifier circuit is
constituted ~~of~~ by a P-channel MOSFET and an N-channel MOSFET
which are formed in the same process as MOSFETs which
constitute the input circuit and the output circuit. ~~which~~
~~are operated upon receiving a power source voltage supplied~~
~~from the external terminal.~~

13. (Currently Amended) A semiconductor integrated
circuit device according to claim 11, ~~wherein~~ further
comprising an internal circuit,

wherein ~~the~~ an internal voltage is formed by reducing
the power source voltage supplied from the second external
terminal, and

the internal circuit is formed with a minimum forming
size of a CMOS processing.

14. (Currently Amended) A semiconductor integrated circuit device according to claim 11, ~~wherein further~~
comprising a ~~the~~ power source circuit,

wherein the power source circuit includes a booster circuit and a negative voltage generating circuit which are operated at a constant voltage formed by using the reference voltage, and

~~a voltage which is~~ voltages formed by the booster circuit and the negative voltage generating circuit ~~is~~ are outputted as a gate drive voltage ~~for driving to drive a~~
liquid crystal, a source drive voltage corresponding to image data, and a liquid crystal common electrode drive voltage.

15. (Currently Amended) A semiconductor integrated circuit device according to claim 7,

wherein the first conductive-type is a p-type and the second conductive-type is an n-type, and

[[a]] wherein the power source voltage ~~which is~~ supplied from the second external terminal is [[a]] positive. ~~power source voltage.~~

16. (Currently Amended) A semiconductor integrated circuit device according to claim 8,

wherein the first conductive-type is a p-type and the second conductive-type is an n-type, and

[[a]]wherein the power source voltage ~~which is supplied~~ from the second external terminal is [[a]] positive. ~~power source voltage.~~

17. (Currently Amended) A semiconductor integrated circuit device according to claim 15,

wherein the second transistor is constituted ~~of~~ by one unit transistor, and

wherein the first transistor is constituted by connecting a plurality of unit transistors corresponding to the second transistor in parallel.

18. (Currently Amended) A semiconductor integrated circuit device according to claim 16,

wherein the second transistor is constituted ~~of~~ by one unit transistor, and

wherein the first transistor is constituted by connecting a plurality of unit transistors corresponding to the second transistor in parallel.